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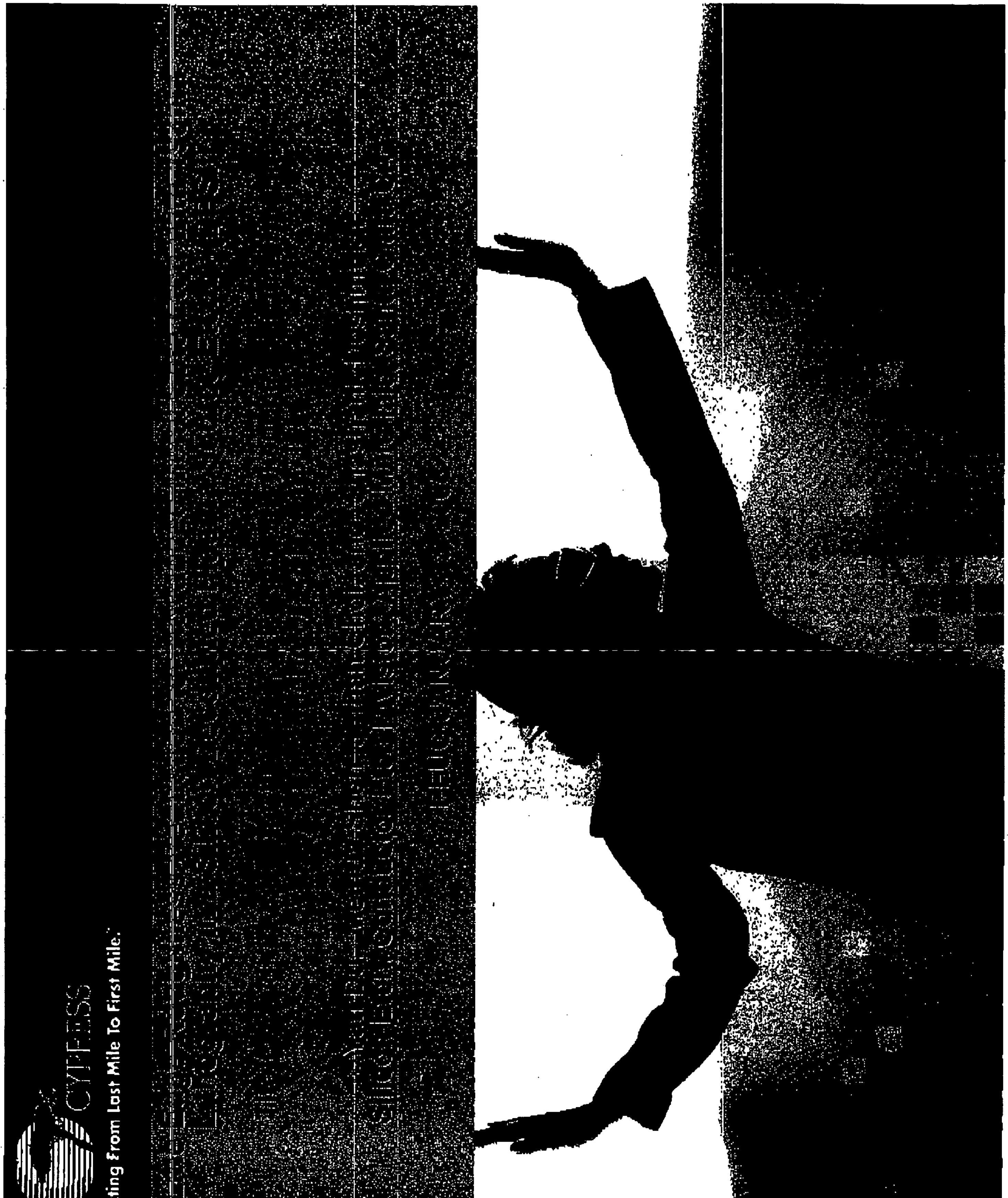

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AVS'04

- What is LER
- Why is LER Important
- How is LER measured
- Modulation of LER from Etch Standpoint
  - Gate
  - STIE
- DPSII hardware & design features
- Hard mask open process
  - 193nm and 248nm PR comparison
  - Mechanism for sidewall striation
  - Etch chemistry and process trends
- W/poly gate etch
  - W gate etch mechanism
  - W etch process trends
- Advanced Gate Etch Challenges
  - Gate Stack complexities
- Current results
- Summary and Conclusions
- Acknowledgements & References

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LER Importance:

- Spend considerable amount from CD budget
- Deteriorates single device performance
- Creates in In-homogeneous performance between devices
- All the above scales as: $\sim LER/CD$

LER measurement:

- Currently done by CD-SEM or AFM
- Involve Image grab and off-line data analysis

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Importance of LER from Device Standpoint

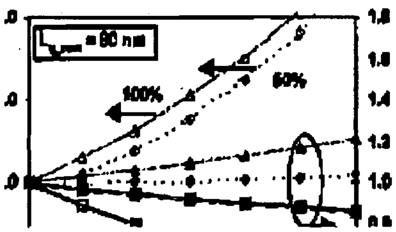
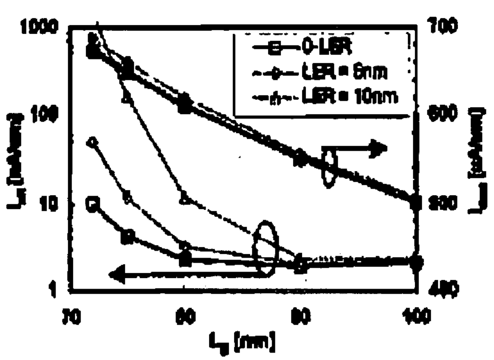


Fig. 1. LER impact on off-state leakage and drive current normalized to a perfect device with 0-LER, i.e., no gate-edge roughness.

LER [nm]

TABLE I
LER REQUIREMENTS AS A FUNCTION OF TECHNOLOGY GENERATION

Technology Generation	Nominal L_g [nm]	LER [nm] Short-range	Long-range
0.18 µm	130	4.1	4.8
0.15 µm	110	3.6	4.5
	80	2.8	3.5
	50-60	1.7	2.1



. 2. Model projection for nMOSFET off-state leakage and drive current as ction of gate length in a 0.13-µm CMOS technology with varying degrees .ER. All technology dependent parameters such as I_s, η, and v_s have been sted to fit the 0.13-µm technology with 80-nm nominal gate length devices 17-Å gate oxides [5].

TABLE II
LER FOR 100-nm RESIST LINES

Lithography approach	Short range LER [nm]	Long range LER [nm]
193 BIM	3.3	9.3
248 APSM	5.9	6.5
248 Alt PSM	3.5	4.1

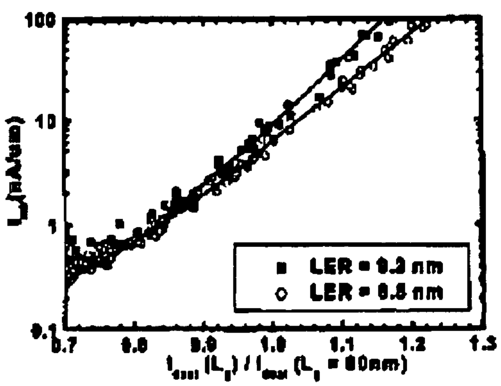


Fig. 3. Gate LER (long) impact on off-state leakage versus drive current figure-of-merit (FOM) for devices with 17-Å gate oxides. Devices were processed in the same lot but with different patterning schemes. I_{off} improvement at constant I_{dsat} is ~1.5x at nominal L_g of 80 nm and becomes 2x at L_g ~ 70 nm. These values compare well with the 2x @ 80 nm and 3x @ 70 nm analytical model predictions for the corresponding gate patterning processes.

* IEEE Electron Devices June 2001 Diaz et al.

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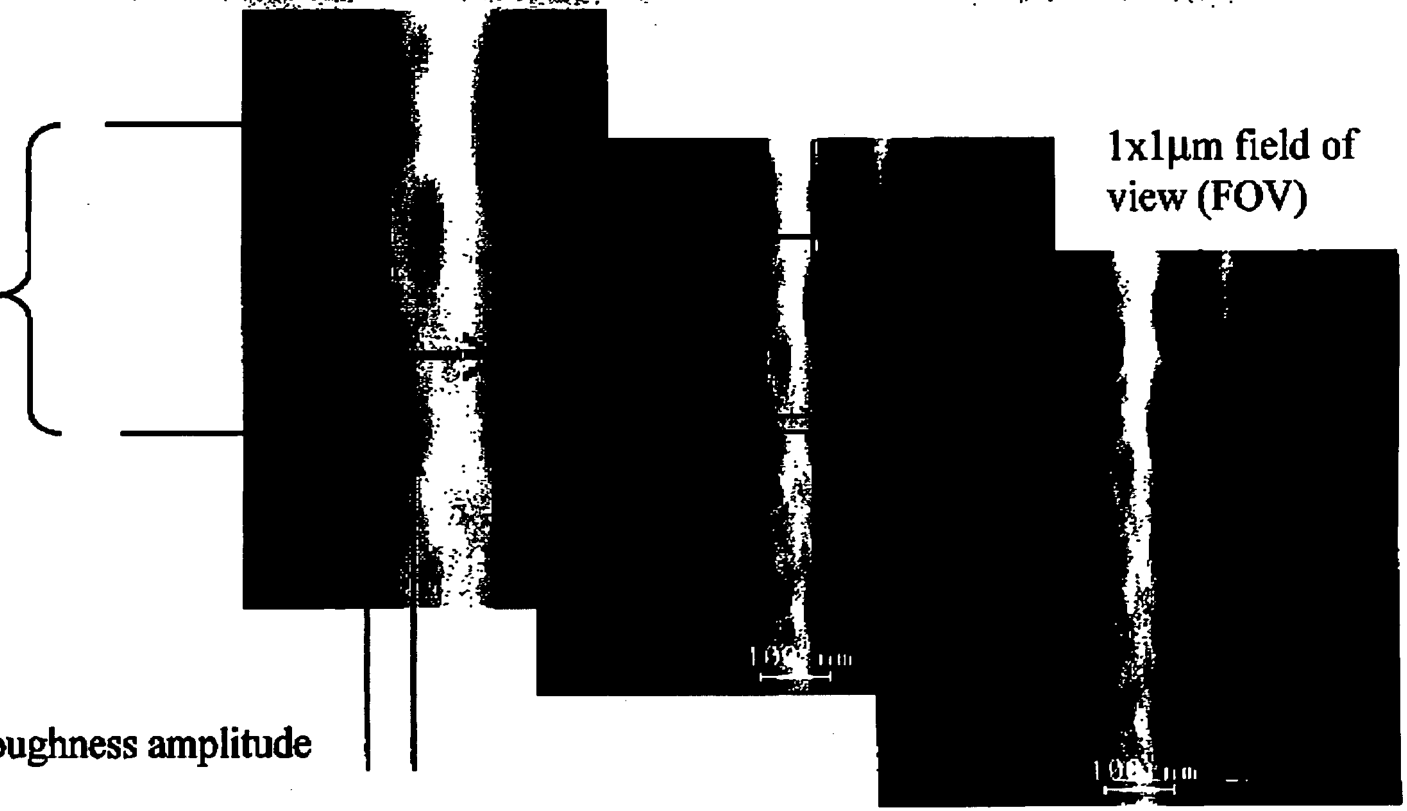

1x1µm field of view (FOV)

Roughness spatial wavelength

Roughness amplitude

Left tilt image of 193 nm resist line

eported roughness: $\boxed{LER = 3(\sigma^2_{left} + \sigma^2_{right})^{0.5}}$

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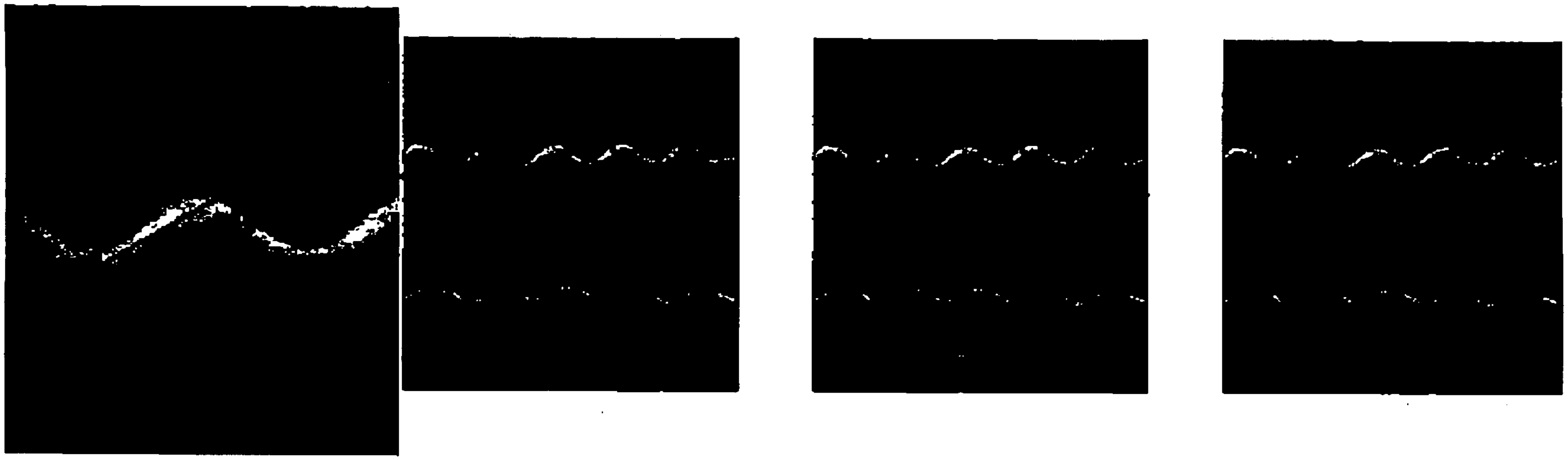
Line Edge Roughness Spatial Wavelength Measurement



eated CD measurement with decreasing measurement boxes width and track the LER litude

the measurement box width decreases below the wavelength of a given roughness ponent, this component no longer contributes and the roughness amplitude decreases.

ce the number of line-scans is constant, the resolution of the measurement increase, and ort roughness components may emerge.

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- PR Type
  - 193nm or 248 nm PR
- PR Thickness
  - Incoming
  - PR selectivity to Etch
- Etch condition
  - Chemistry
  - Etcher H/W

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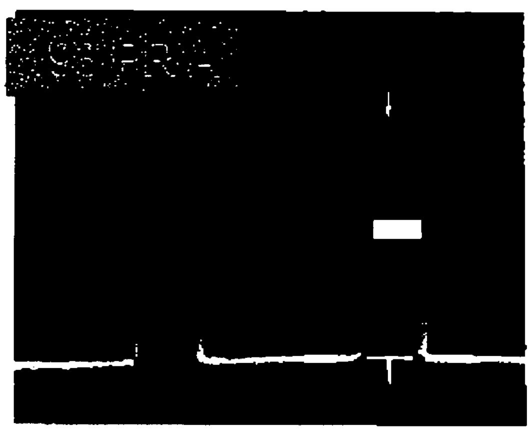
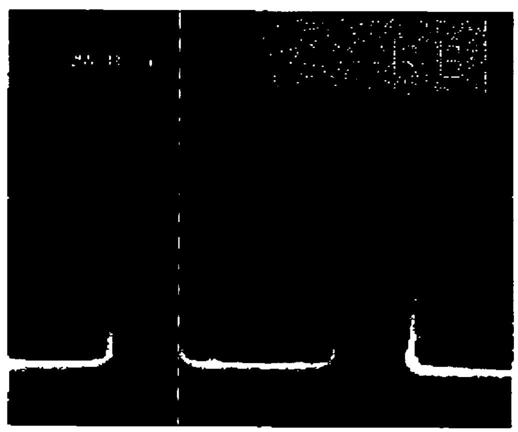
PR loss ~ 1800 A for both 248 nm and 193 nm PR For CHF3/CF4 chemistry





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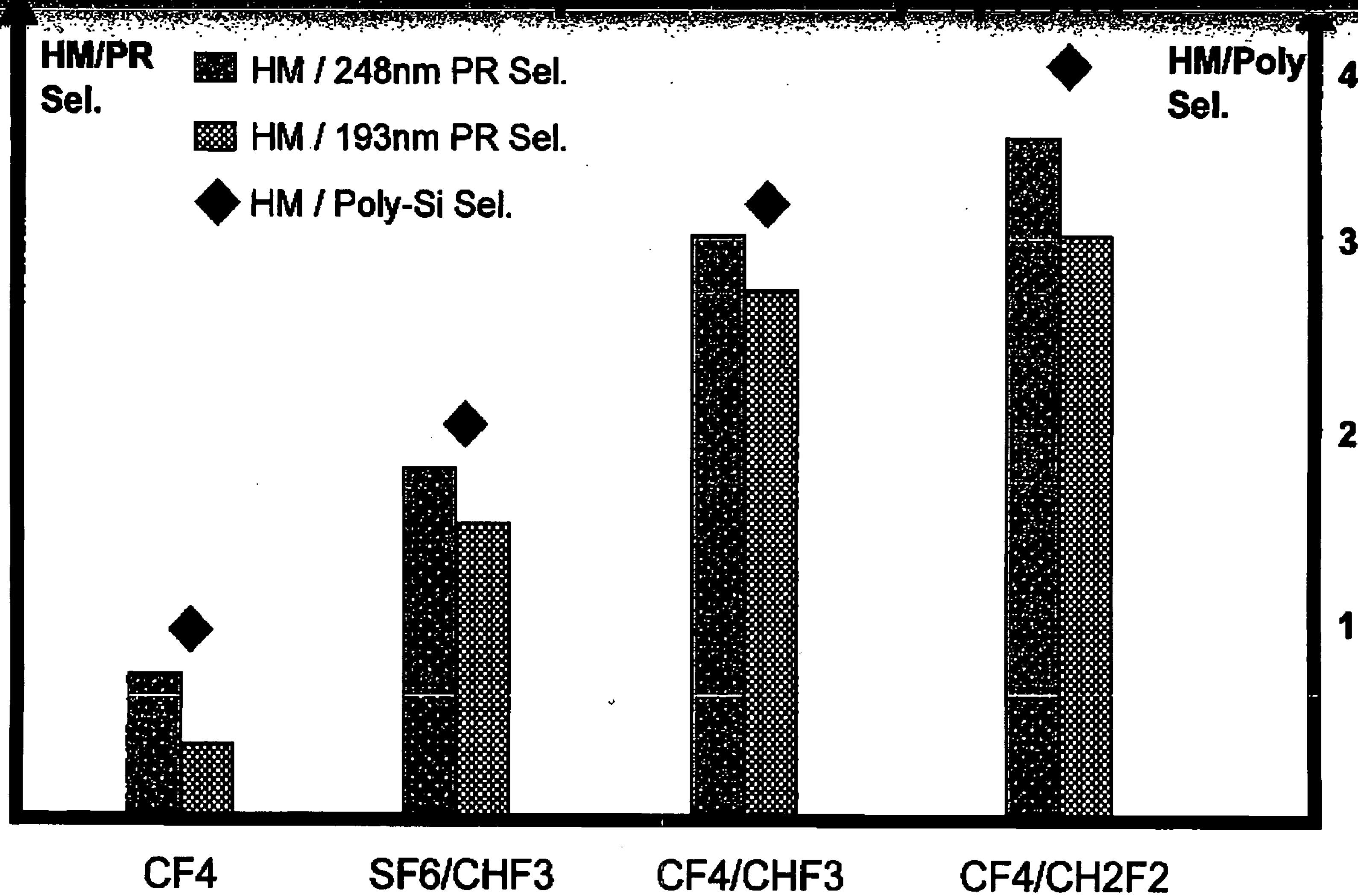

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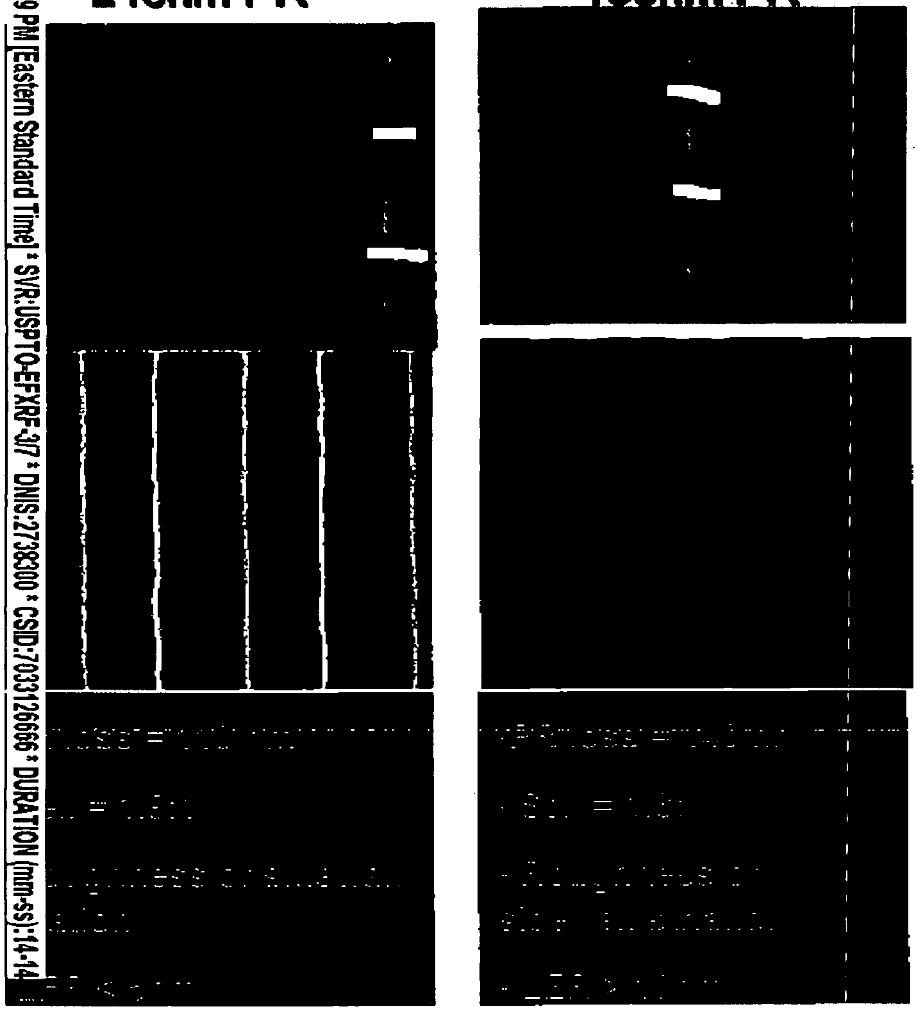
248nm PR

193nm PR



- CF4/CH2F2 chemistry
- High selectivity to resist can be achieved due to CFx polymer passivation
- Severe line edge roughness (LER) or sidewall striation is observed on 193nm PR patterned wafer while 248nm patterned wafer etched by the same process shows smooth sidewalls
- Note that sidewall striation is not caused by poor resist selectivity although LER can sometimes be associated with insufficient resist selectivity

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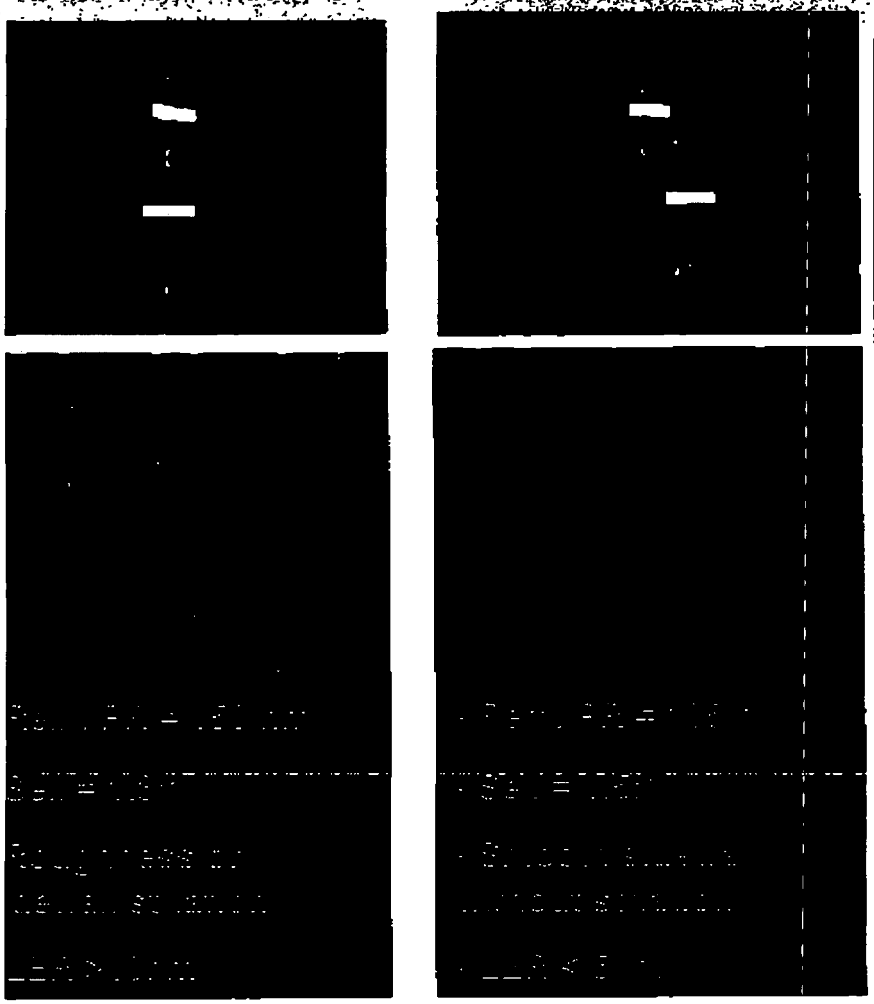
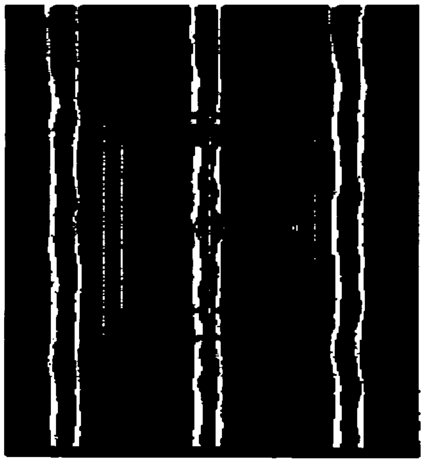


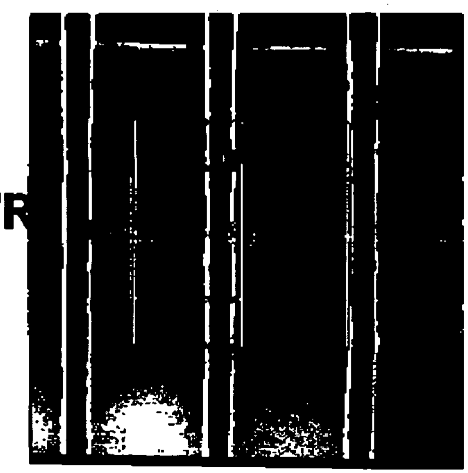
- Same 193nm patterned wafers display completely different signatures using different HM etch chemistries
- Possible mechanism: The physical strength of CFx based passivating polymer may be proportional to F/C ratio. [1]
- Strength of amorphous carbon can be enhanced dramatically by fluorinating
- "Tougher" passivation layer for CHF3 chemistry is harder to be redefined by ion bombardment and thus results in smooth sidewalls

Reference: [1] T. Miyamoto et al, J. Vac.Sci.Technol. B 9(2), Mar/Apr 1991

m LWR



nm LWR



- Same 193nm patterned wafers display completely different signatures using different ARC etch chemistries
- Observation: Non Carbon based ARCE much smoother
- LWR reduces from 8 nm to 3 nm with change in ARC etch chemistry for 65 nm Gate etch process.

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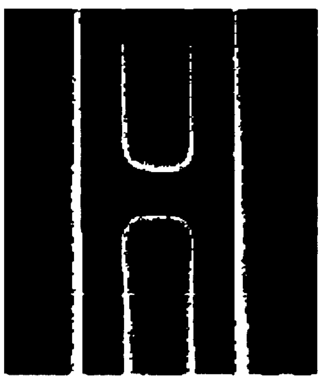
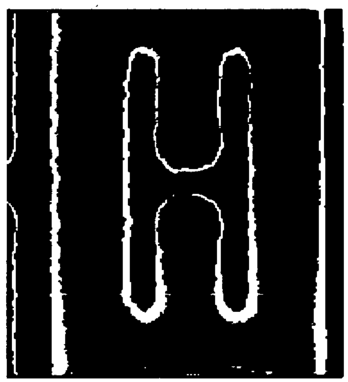
Technology	Resist	FOM LER (nm)	STIE LER (nm)	Recipe
0.25um	248	6	6	MERIE old
0.1um	193	5	14	MERIE old
0.1um	193	5	9	MERIE new
0.1um	193	5	6.5	DPS

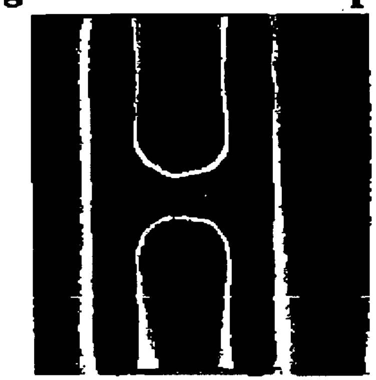
TIE Mask open uses CHF3/CF4 Process for all splits

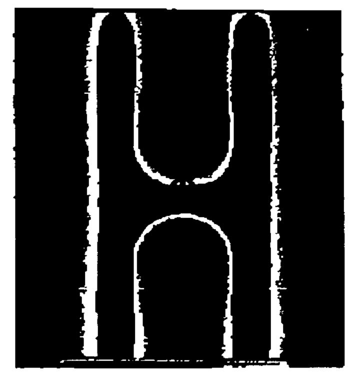
TIE LER Depends on

- Resist type (6nm for 248 → 14 nm for 193nm using same etch conditions)
- Etch Process conditions modulates LER on same etcher. (14 nm→ 9 nm)
- 193 and 248 LER performance matched using new Etcher with optimized condition









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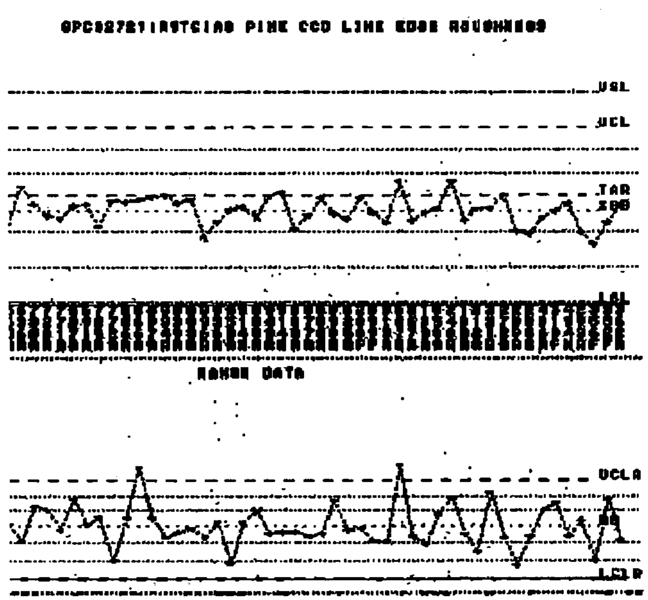
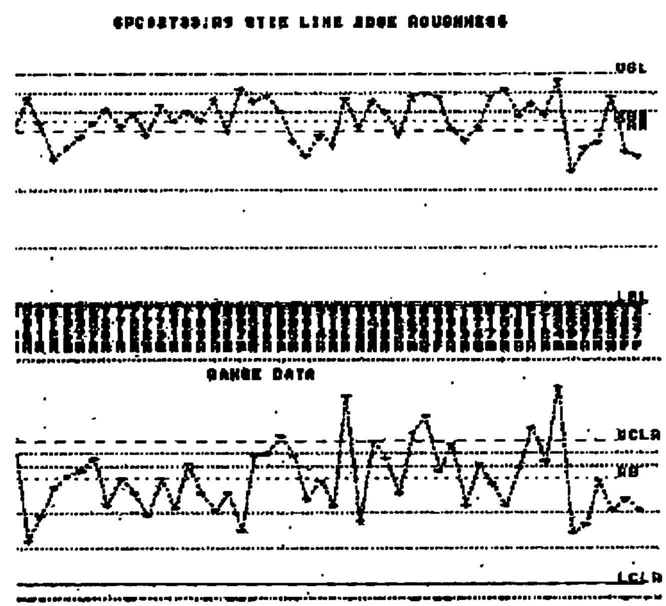


P1ME on DPS



STIE on MERIE

Avg. LER using MERIE higher than ICP type reactor by 50 %

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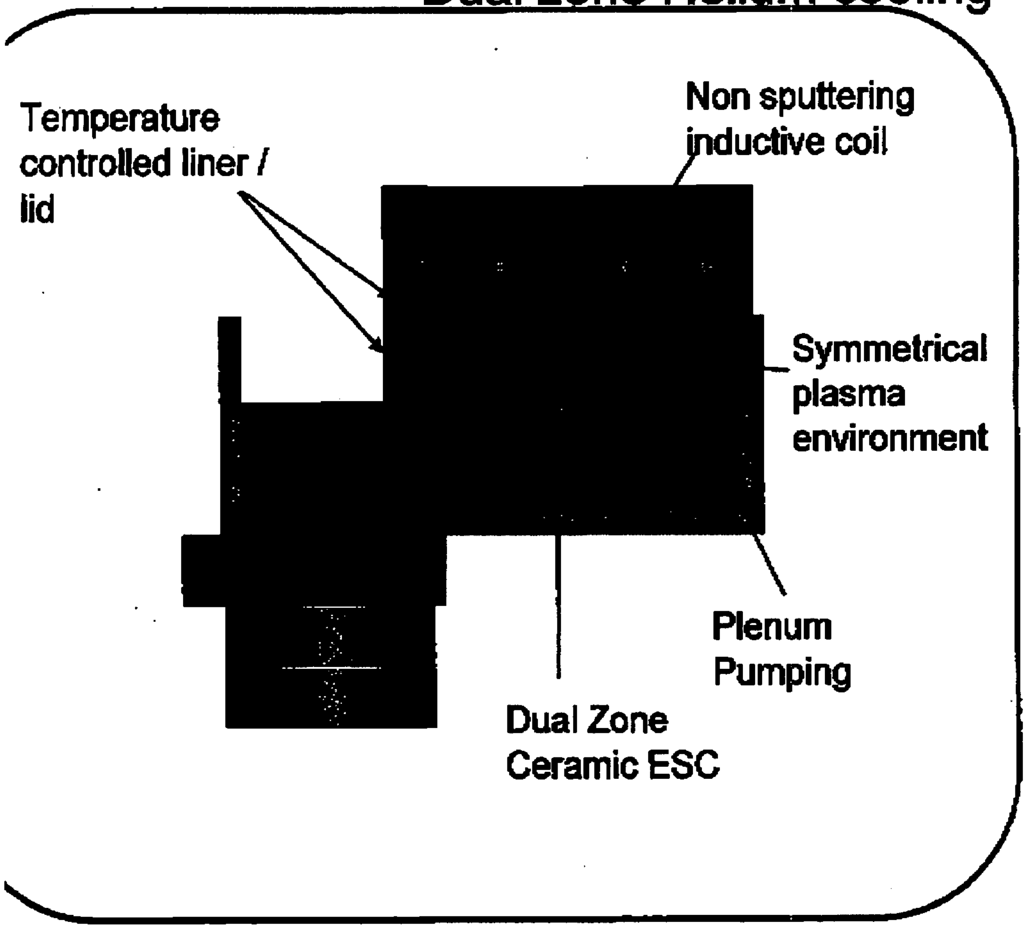
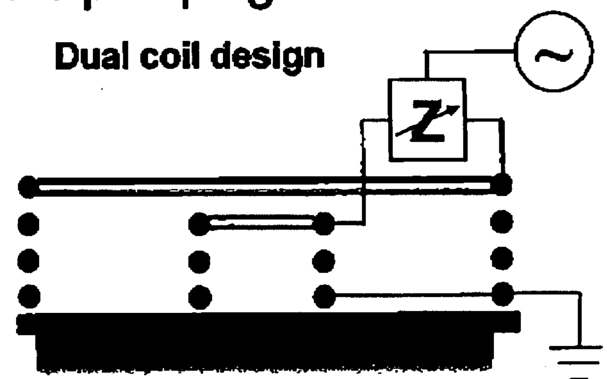
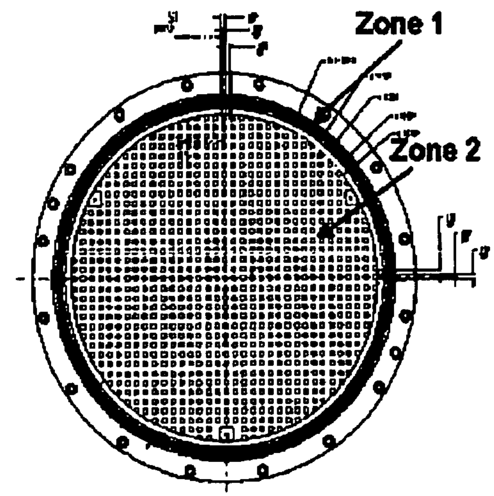
– Dual source coil design
– Center gas feed with symmetric pumping
– Dual zone Helium cooling



Dual coil design





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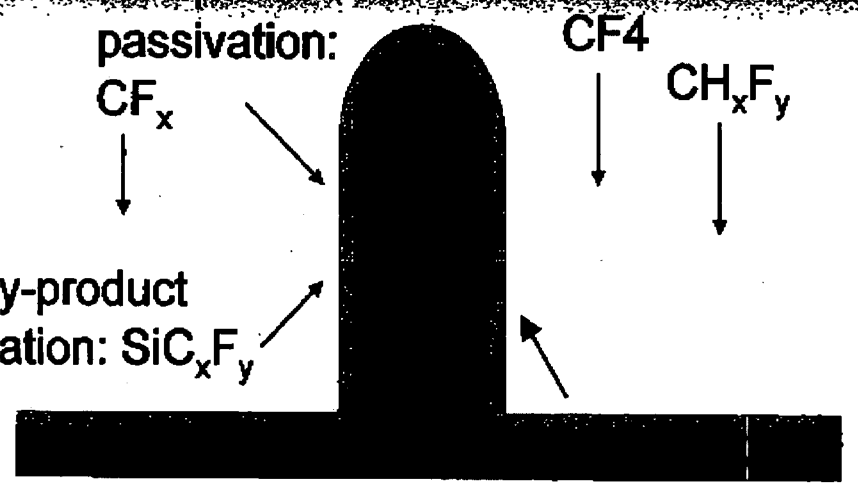

...triation Formation Mechanism:

...tep1: As etching progresses, polymer builds up ...luorinated amorphous carbon) on the resist sidewalls

...tep 2: Depending on the polymer strength, ion ...ombardment causes non-uniform polymer removal

...tep 3: The non-uniform polymer layer results in rough ...esist sidewalls

...tep 4: The striated resist pattern is then transferred down to ...e underlayers

Sidewall striation formation depends on:

- Resist material
- Etch chemistry
- Power regime

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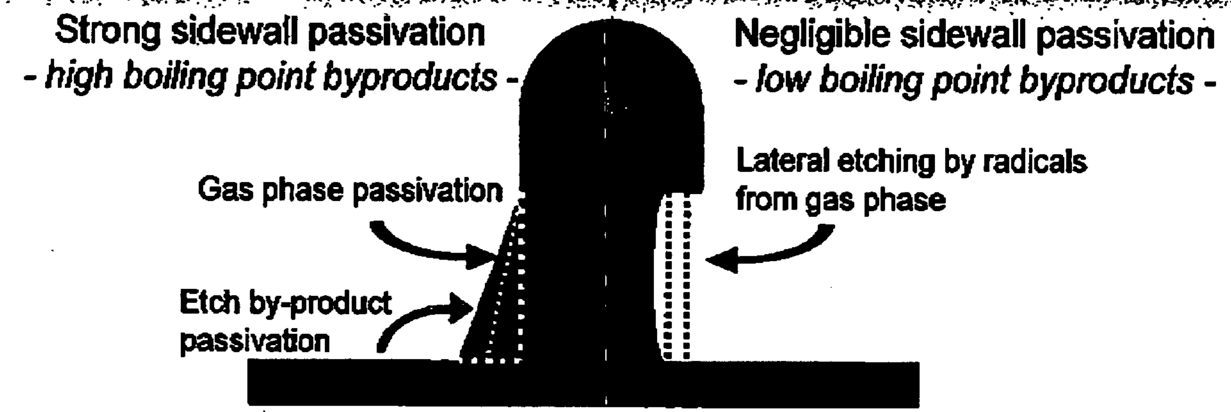

Fluorine Etchants

…SF_6 - high etch rate, inexpensive, increased …ateral etching, small process window, clean

…NF_3 - high etch rate, expensive, good sidewall …assivation, large process window, clean

…CF_4 - slow etch rate, inexpensive, reduces …oughness

	SF_6 based	CF_4 based	NF_3 based
W/Poly Selectivity	0.3-0.4	<0.5 (very slow)	>4
	SF_6 based	CF_4 based	NF_3 based
W/WN$_x$ Selectivity	0.9-1.4	<0.5	0.8-1.4
	SF_6 based	CF_4 based	NF_3 based
W/TiN$_x$ Selectivity	>4	—	>4

Passivants

N_2, Cl_2, CF_4, O_2

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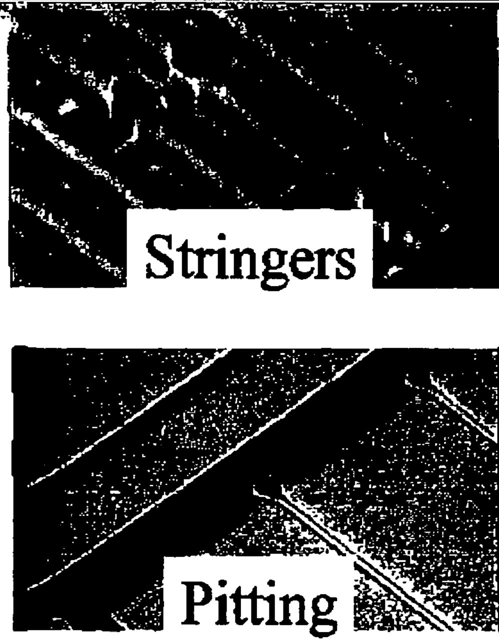
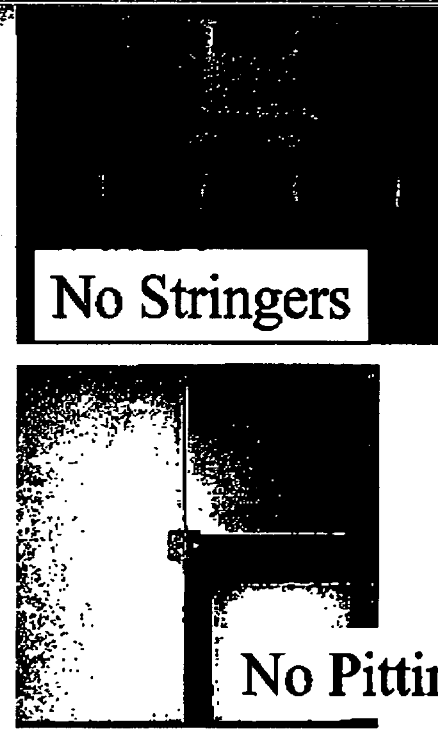


SF_6 Based W Chemistry



NF_3 Based W Chemistry

SF6 versus NF3 based W etch

- SF6 chemistry provides acceptable profile performance but poor etch rate uniformity and severe etch rate micro-loading. Stringers and pitting seen on the same wafer for different loading areas. Screening splits show NF3 best choice for W etch.

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Metal-Gate Stack Complexities

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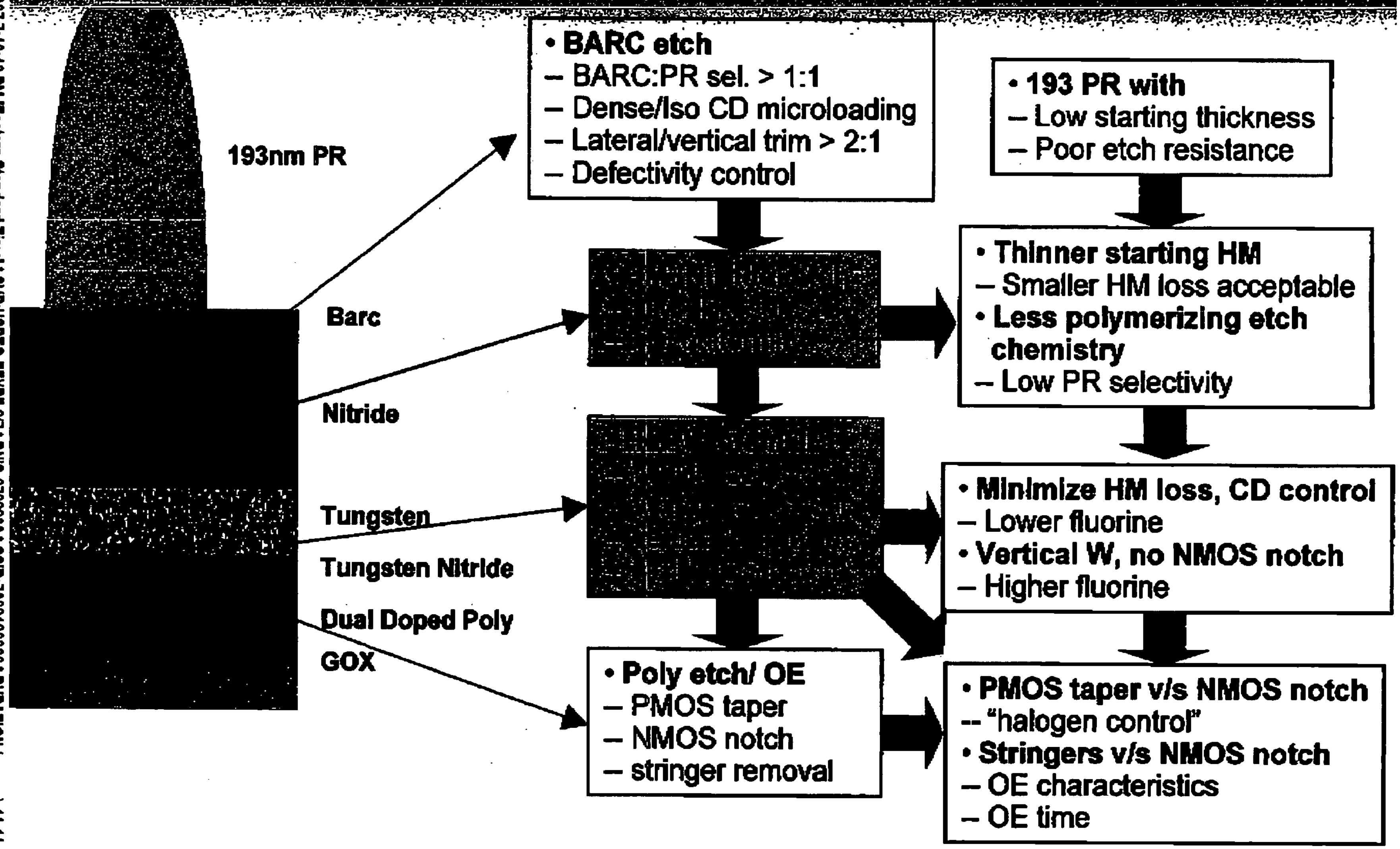

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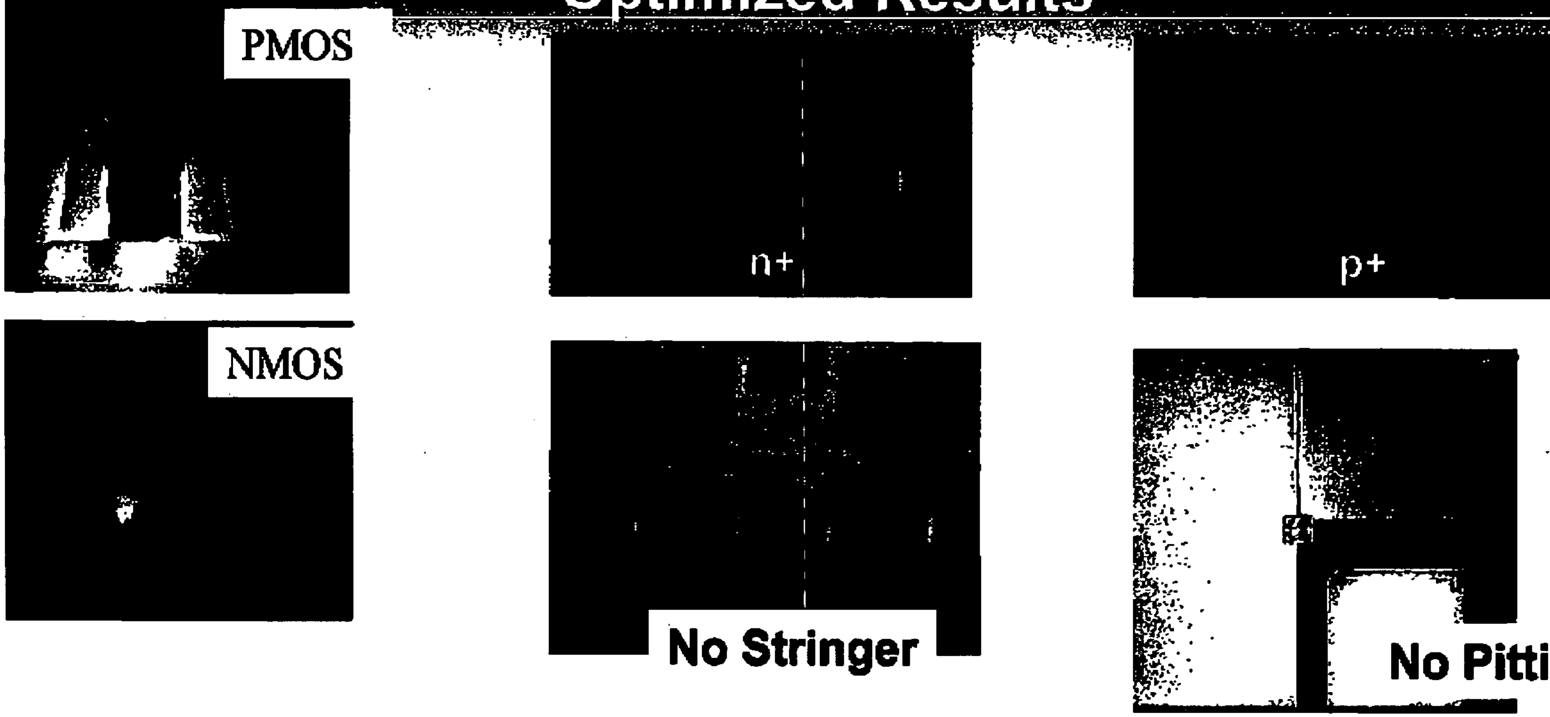
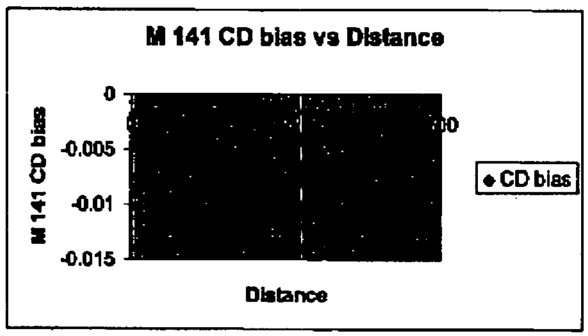
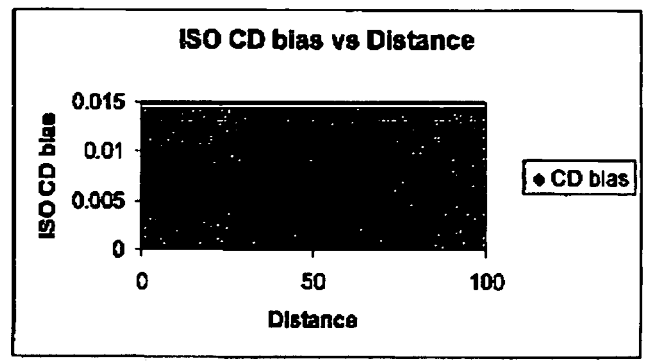
Optimized Results



emaining HM adequate
/ Profile: >87
oly Profile: >89
pacer in TEM unoptimized





- 193 nm PR more susceptible to LER than 248nm.
  - 193 nm resist is Acrylic based polymer compared to 248 nm resist which is Aromatic based polymer, therefore 193 resist is more susceptible to etch conditions.

- Etch conditions is a significant modulator of LER
- 193 nm can perform equivalent to 248 for STIE and Gate as long etch conditions and etcher H/W regime optimized.
- PR Thickness
  - 193 nm PR thinner than 248. This makes LER more challenging.
  - Thinner PR remaining after etch makes LER worse.
  - PR selectivity from Etch for 193 and 248 depends on etch process condition. Can be made equivalent.

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Cypress R&D

- Chris Seams, Shahin Sharifzadeh, Albert Bruggerman, Harry Lee, Itzhik Gilboa, Jeff Watts, Geetha Narashiman, K. Ramkumar, Alain Blosse, Kiyoko Ikeuchi, Chris Jones, My Thang, Helena Stadniychuk, Peter Keswick, Dan Arnzen, Craig Whichard, Mike Moore, Dick Duvall, Phil Mcgowan, Pete Roth, Robin Van den Neiwzhen, Oliver Pohland, Ravi Kapre, Wade Xiong

Applied Materials Silicon Etch division

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Applied Materials North America Regional Support

- Eric Lim, Kolan Saravanan, Kamatchi Subramaniam, Leonard Moravek, Paul Arleo, Danny Xiong, Ed Laughlin, Brent Riggs, Joe Farrah, Frank Sekera

References

- *"An Experimentally Validated Analytical Model For Gate Line Edge Roughness (LER) Effects on Technology Scaling", Diaz IEEE Electron Device Letters Vol. 22 No.6 June 2001*

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